Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1.(currently amended) ~~Method~~ A method for communication between an IC (integrated circuit) and an external RAM (random access memory) ~~DRAM~~, where the external RAM ~~DRAM~~ has at least one memory bank and ~~communicates with~~ communication between the IC and the external RAM is performed via two or more channels, where data exchange between the IC and the external RAM necessitates at least two memory bank commands, ~~wherein~~ the method comprising:

transmitting ~~transmissions of~~ memory bank commands [[of]] via multiple channels;

prioritizing the transmitted memory bank commands ~~are prioritized~~ on the basis of a static priority allocation; and

further prioritizing ~~for commands and~~ the commands having the same static priority ~~are further prioritized~~ on the basis of a dynamic priority allocation for the channels.

2.(currently amended) The method ~~Method~~ according to Claim 1, wherein the prioritizing the transmitted memory bank commands on the basis of a static priority allocation includes: ~~static priority allocation for commands involves~~

giving a 'Burst Terminate' command ~~being given~~ the highest priority,

giving a 'Read' or 'Write' command ~~being given~~ the second highest priority,

giving an 'Activate' command ~~being given~~ the third highest priority, and

giving a 'Precharge' command ~~being given~~ the lowest priority.

3.(currently amended) The method ~~Method~~ according to Claim 1, wherein the prioritizing the commands having the same static priority on the basis of a dynamic priority allocation for the channels includes:

~~dynamic priority allocation for channels involves a channel being given the lowest priority after~~ giving the lowest priority to a channel via which a command has been sent.

4.(currently amended) The method ~~Method~~ according to Claim 1, wherein the prioritizing the commands having the same static priority on the basis of a dynamic priority allocation for the channels includes:

~~dynamic priority allocation involves~~ giving one of the channels ~~being given~~ the highest priority in the next clock cycle if [[it]] this channel does not have the highest priority in the current clock cycle and a command is sent via another channel ~~sends a command~~.

5.(currently amended) The method ~~Method~~ according to Claim 1, wherein the prioritizing the commands having the same static priority on the basis of a dynamic priority allocation for the channels includes:

withdrawing ~~dynamic priority allocation involves one of the channels losing~~ the highest priority of a channel only when [[it]] this channel can send a command.

6.(currently amended) The method ~~Method~~ according to Claim 1, wherein the method further includes accessing ~~channels access~~ physically separate memory areas in the external RAM via the channels ~~DRAM~~.

7.(currently amended) The method ~~Method~~ according to Claim 1, wherein the method further includes accessing ~~channels access~~ jointly used memory areas in the external RAM via the channels ~~DRAM~~ and the assurance is given that no successive access operations to a jointly used memory area will arise.

8.(currently amended) The method ~~Method~~ according to Claim 1, wherein the method further includes accessing various memory banks via at least one

channel by a network ~~is provided which allows at least one channel to access various memory banks~~.

9.(currently amended) The method ~~Method~~ according to Claim 1, wherein the method further includes always having an access operation to another memory bank effected between two access operations to a memory bank ~~always have an access operation to another memory bank effected between them~~.

10.(currently amended) The method ~~Method~~ according to Claim 1, wherein the method further includes permitting two successive access operations to a memory bank ~~are permitted~~ when [[they]] the access operations are made to the same row in the memory bank.

11.(currently amended) The method ~~Method~~ according to Claim 1, wherein the method further includes depicting the states of the memory banks ~~are depicted~~ by associated state machines.

12.(currently amended) The method ~~Method~~ according to Claim 1, wherein the method further includes using a plurality of RAM ~~DRAM~~ modules ~~are used~~ and transmitting a chip enable signal ~~is transmitted~~ in order to select the desired module.

13.(currently amended) ~~Memory~~ A memory controller for an IC (integrated circuit) with an external RAM (random access memory) ~~DRAM~~, where the external RAM ~~DRAM~~ has at least one memory bank and ~~communicates with~~ communication between the IC and the external RAM is performed via two or more channels, where data exchange between the IC and the external RAM necessitates at least two memory bank commands, the memory controller comprising:

~~wherein it has~~ a command scheduler which prioritizes [[the]] transmissions of memory bank commands of multiple channels on the basis of a

static priority allocation for commands and the commands having the same priority are further prioritized by the command scheduler on the basis of a dynamic priority allocation for the channels.

14.(currently amended) ~~Appliance~~ An appliance for reading and/or writing to storage media, wherein the appliance comprising a memory controller utilizing the method according to Claim 1.